BMS COLLEGE OF ENGINEERING, BENGALURU-19
Autonomous Institute, Affiliated to VTU
Department of Electronics and Communication Engineering

Scheme and Syllabus
M. Tech (VLSI Design and Embedded systems)
Batch 2018 onwards

Web: www.bmsce.ac.in

Vision of BMS College of Engineering

Promoting Prosperity of mankind by augmenting human resource capital through Quality Technical Education & Training

Mission of BMS College of Engineering

Accomplish excellence in the field of Technical Education through Education, Research and Service needs of society

Vision of Electronics and Communication Department

To emerge as a center of academic excellence in electronics, communication and related domains through knowledge acquisition, knowledge dissemination and knowledge generation meeting global needs and standards.

Mission of Electronics and Communication Department

Imparting quality education through state of the art curriculum, conducive learning environment and research with scope for continuous improvement leading to overall professional success.

PROGRAM EDUCATIONAL OBJECTIVES

The department has, defined the following PEOs for the PG programme in VLSI Design & Embedded system.

PEO1:

PEO1: Graduates shall be capable of building their career in industries, R&D establishments as well as in academia in the domain of VLSI Design and Embedded systems.

PEO-2:

PEO2: Graduates shall be capable of conducting research leading to technology solutions of societal importance.

PEO-3:

PEO3: Graduates shall collaborate, manage and execute projects in teams using relevant tools/technologies and demonstrate professional behavior.

PROGRAM OUTCOMES

Program Outcomes (POs), are attributes acquired by the student at the time of graduation. These attributes are measured at the time of Graduation, and hence computed every year for the outgoing Batch. The POs are addressed and attained through the Course Outcomes (COs) of various courses of the curriculum.

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

Distribution of credits

Category	No of Credits
Program Core Course	26
Program Elective Course	15
All programme core Course	02
Open Elective Course	04
Internship	9
Technical Seminar	04
Audit Courses	2 units
Project Work	28

Total Number of Credits (I Sem – IV Sem) = 88 Credits

Distribution of Marks

For each subject CIE will be conducted for 50, SEE for 100 (will be reduced to 50) and hence total marks of 100 are allotted to each subject including CIE(50) and SEE (50)

M. Tech. (VLSI Design and Embedded systems)

I Semester **CREDIT BASED**

Subject Code	Course Title	CREDITS			
		L	T	P	
18ECVEBSAM	Applied Mathematics	3	0	0	3
18ECVEPCDI	Digital IC design	3	0	1	4
18ECVEGCES	Advanced Embedded System	3	0	1	4
18ECVEPCAI	Analog IC design	3	0	0	3
18ECVEPEZZ	Elective -1	3	0	0	3
18ECVEPEZZ	Elective -2	3	0	0	3
18ALLPICRM	Research Methodology	2	0	0	2
Total		20	0	2	22

Note: Two electives to be chosen from the list below:
Elective will be offered for a minimum strength of six candidates (out of 18) / eight candidates (out of 24)

Elective -1 and Elective -2			
18ECVEPEST	Static Timing Analysis	18ECVEPELP	Low Power VLSI Design
18ECVEPECA	Advanced Computer Architecture	18ECVEPEEC	Embedded Computing and Networking
18ECVEPEMP	Device Modeling and Processing Technology	18ECVEPEAV	Advances in VLSI Structure

Note: (i) The Course Code Expansion: Ex.: 18ECVEBSAM: 18 = Year of syllabus introduced / revised, EC = Dept., VE = Program, BS = Basic Science, AM = Advanced Mathematics.

PC/PE: Program Core / Program Elective, GC/GE: Group Core / Group Elective, OE: Open Elective.

ZZ (course abbreviation of Electives),

(ii) Exception for 18ALLPICRM: ALLP = All Program, I = Institution C = Core, RM = Research Methodology.

M. Tech. (VLSI Design and Embedded systems)

II Semester **CREDIT BASED**

Subject Code	Course Title	CREDITS			
		L	T	P	
18ECVEPCMS	Mixed Signal Circuit Design	3	0	1	4
18ECVEPCDT	Design for Testability	3	1	0	4
18ECVEGCRT	Real Time Operating Systems	3	0	1	4
18ECVEPEZZ	Elective -3	3	0	0	3
18ECVEPEZZ	Elective -4	3	0	0	3
18ECVEOEZZ	Open Elective	4	0	0	4
Total		19	1	2	22

Note: Two electives to be chosen from the list below:
Elective will be offered for a minimum strength of six candidates (out of 18) / eight candidates (out of 24)

Elective -3 and Elective -4			
18ECVEPESV	System Verilog and verification	18ECVEPEPD	Physical Design
18ECVEPEHS	Hardware-Software Co-design	18ECVEPEAA	Embedded Design using ARM Architecture
18ECVEPESC	System On Chip Architecture	18ECVEPEMD	Memory Design and Testing

Open Elective	
18ECVEOEMM	MEMS and Micro Systems

M. Tech. (VLSI Design and Embedded systems)

III Semester **CREDIT BASED**

Subject Code	Course Title	CREDITS			
		L	**T**	**P**	
18ECVEGEZZ	Elective 5	2	1	0	3
18ECVEPWP1	Project Work- Phase-1	0	0	8	8
18ECVEPCIN	Internship	0	0	9	9
18ECVESR01	Technical Seminar-1	0	0	2	2
18ECVENCA1	Audit Course-1	0	0	0	2 UNITS
Total		0	0	22	22

Elective 5			
18ECVEGEUV	UVM Methodology concepts	18ECVEGESL	Introduction to scripting languages

M. Tech. (VLSI Design and Embedded systems)

IV Semester **CREDIT BASED**

Subject Code	Course Title	CREDITS			
		L	**T**	**P**	
18ECVESR02	Technical Seminar-2	0	0	2	2
18ECVEPWP2	Project Work Phase-2	0	0	20	20
18ECVENCA2	Audit Course-2	0	0	0	2 UNITS
Total		4	0	20	22

Applied Mathematics

COURSE CODE	18ECVEBSAM	COURSE TITLE	Applied Mathematics
CREIDTS	3	L-T-P	3-0-0

Course Outcomes and POs addressed:

At the end of this course, student shall be able to:

CO-No	Course Outcomes	PO
CO1	Demonstrate knowledge and understanding of the underlying concepts of random variables and stochastic processes	PO3
CO2	Demonstrate knowledge of the mathematical concepts and computational aspects of linear algebra and graph theory	PO3
CO3	Analyse domain related engineering problems and develop analytical problem solving approach making use of the theoretical concepts	PO3

Syllabus:

Module 1:
Review of basic probability theory. Definition of random variables and probability distributions, probability mass and density functions, expectation operator, illustrative examples (8 hrs)

Module 2:
Moments, central moments, characteristic functions, probability generating functions - illustrations Poisson, Gaussian and Erlang distribution examples. Pair of random variables – Joint PMF, PDF, CDF. (7 hrs)

Module 3:
Random Processes - Classification. Stationary, WSS and ergodic random process. Auto-correlation function-properties, Gaussian random process, Engineering Applications of Random processes. (6 hrs)

Module 4:
Linear Algebra: Introduction to vector spaces and sub-spaces, definitions, illustrative example. Linearly independent and dependent vectors- Basis-definition and problems. Linear transformations-definitions, Matrix form of linear transformations - Illustrative examples, Computation of Eigen values and Eigen vectors of real symmetric matrices - Given's method. (8 hrs)

Module 5:

Computational Graph Theory: Graph enumerations and optimization: DFS-BFS algorithm, shortest path algorithm, min-spanning tree and max-spanning tree algorithm, basics of minimum cost spanning trees, optimal routing trees, optimal communication trees, network flow algorithms (7 hrs)

Text Books:

1. S L Miller and D C Childers**, "Probability and random processes: application to signal processing and communication**", Academic Press / Elsevier 2004.

2. David C. Lay, "**Linear Algebra and its Applications**", 3rd Edition, Pearson Education, 2003.

3. Geir Agnarsson and Raymond Greenlaw "**Graph Theory- Modeling, Applications and Algortihms",** Pearson Education, 2007.

Reference books:

1 A. Papoulis and S U Pillai, **"Probability, Random variables and stochastic processes",** McGraw Hill 2002

2 Roy D. Yates and David J. Goodman, **Probability and Stochastic Processes: A friendly introduction for Electrical & Computer Engineers**/

3. MIT Open courseware**, Introduction to Linear Algebra, Course 18.06**

4 Nausing Deo, "**Graph Theory with applications to Engineering and Computer Science**", Prentice Hall of India, 1999.

Digital IC Design

COURSE CODE	18ECVEPCDI	COURSE TITLE	Digital IC Design
CREIDTS	4	L-T-P	3-0-1

CO-No	Course Outcomes	PO
CO1	Design**,** write program and simulate Static and Dynamic circuits to meet the specification	PO3
CO2	Analyse the given circuit to arrive at the specification	PO3
CO3	Engage in literature survey in a group on the topic related to course and submit a detailed report	PO2

Prerequisite: The Metal Oxide Semiconductor (MOS) Structure, MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects.

Module 1

Static Characteristics of MOS Inverters: Resistive load inverters, CMOS Inverter.

Module 2

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits.

Module 3

Circuit Simulation: Sources and Passive Components, Transistor DC Analysis, Inverter Transient analyses, Sub circuits and measurements, Optimization**,** SPICE Commands, Level 1 model, Level 2 and 3 models, BSIM Models, Design Corners. Other SPICE commands.

Module 4

Principles of RTL Design: Verilog Coding Concepts, Verilog coding guide lines: Combinational, Sequential, FSM. General Guidelines, Synthesizable Verilog Constructs, Sensitivity List, Verilog Events, RTL Design Challenges.

Module 5

Synthesis, Libraries and Technology Mapping: Introduction to synthesis, logical synthesis of combinational and sequential circuits, Synthesis Methodologies, Pre and post synthesis mismatch, Translation, mapping and optimization. Overview of Libraries, design constraints, importance of wire load models.

Reference Books

1. Sung Mo Kang & Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw-Hill, Third Edition.

3. Verilog HDL: A Guide to Digital Design and Synthesis by Samir Palnitkar, 2nd Edition

4. Verilog HDL Synthesis A Practical Primer by J. Bhasker

5. Fundamentals of Digital Circuits by A. Anand Kumar, 2nd Edition

6. Principles of VLSI RTL Design: A Practical Guide by Sanjay Churiwala , Sapan Garg, 2011

Digital IC Design Lab

Lab Work: 2 hrs/week

Course Outcomes:

At the end of the laboratory work, students will be able to:

- Design digital Circuit using CMOS Technology
- Use EDA tools like Cadence, Synopsis, Mentor Graphics and other open source software tools like Ngspice,

List of Experiments:

PART I

1) Use V_{DD}=1.8V for 0.18um CMOS process, V_{DD}=1.3V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.

Input Characteristics Analysis

a) Plot and analyse I_D vs. V_{GS} at different drain voltages for NMOS, PMOS. Determine V_t

b) Plot log I_D vs. V_{GS} at particular gate voltage (high) for NMOS, PMOS and determine I_{OFF} and sub-threshold slope.

Output Characteristics Analysis

a) Plot I_D vs. V_{DS} at different gate voltages for NMOS, PMOS and determine Channel Length modulation factor.

b) Plot I_D vs. V_{DS} at different drain voltages for NMOS, PMOS, plot DC load line and calculate g_m, g_{ds}, g_m/g_{ds}, and unity gain frequency. Tabulate your result according to technologies and comment on it.

2) Use V_{DD}=1.8V for 0.18um CMOS process, V_{DD}=1.2V for 0.13um CMOS Process and V_{DD}=1V for 0.09um CMOS Process.

a) Perform the following

i. Plot VTC curve for CMOS inverter and thereon plot dV_{out} vs. dV_{in} and determine Transition voltage. Calculate V_{IL}, V_{IH}, N_{MH}, N_{ML} for the inverter.

ii. Plot VTC for CMOS inverter with varying V_{DD}.

iii. Plot VTC for CMOS inverter with varying device ratio.

b) Perform transient analysis of CMOS inverter with no load and with load and determine t_{pHL}, t_{pLH}, 20%-to-80% tr and 80%-to-20% tf. (use V_{PULSE} = 2V, C_{load} = 50fF)

c) Perform AC analysis of CMOS inverter with fan-out 0 and fan-out 1. (Use C_{in}= 0.012pF, C_{load} = 4 PF, R_{load} = k)

3) Perform simulation to measure the **power** and **delay** for digital circuits.

PART II

Design, Write Verilog code for the circuits given below, Simulate, synthesize, view report, Use EDA Tools like Cadence, Mentor Graphics, and Synopsis.

1) Adder

2) Magnitude Comparator

3) Parity Generator

4) D and T F/F

4) Universal Shift Register

5) Counter

Advanced Embedded Systems

COURSE CODE	18ECVEGCES / 18ECELGCES	COURSE TITLE	Advanced Embedded Systems
CREIDTS	4	L-T-P	3-0-1

CO-No	Course Outcomes	PO
CO1	Comprehend concepts in the field of Embedded Systems	PO3
CO2	Apply concepts to build Embedded Systems	PO3
CO3	Develop C programs for execution on microcontroller/SOC development board based on ARM architecture. Develop Python programs to interface with Embedded Systems.	PO3
CO4	Engage on market survey of various available Computer/Embedded architecture based on performance, power consumption and pricing criteria.	PO2

Students Prerequisite:
Introduction course on Embedded Systems, Microcontrollers (any)
Basic C Programming Skills

Module 1

Introduction to ARM architecture and Real Time Embedded Systems:
Introduction to ARM Architecture, Difference between Microcontroller, Application Processor and Realtime Processor architectures. Detail study of ARM Cortex-M processor. Introduction to peripheral interface scheme in ARM processors. Operating Modes and Exceptions. Time Management in Embedded Systems. ARM Instruction Set and its features.

Module 2

Embedded C Programming:
Detail study of bitwise operators in C. Arrays, Structures and Unions. Pointers and Dynamic Memory allocation. Pre-processor Directives in C. Modular C programming approach. Relook into data types of C. Memory Map and Storage Classes of C. Storage Type Qualifiers.

Module 3

Python Programming:

Introduction Python Programming, data types, lists, tuples, dictionaries, conditional statements, iterative statements, functions. File and I/O handling, serial device interfaced to external devices. Strings and data formatting, integer, bytes, hexadecimal representation.

Module 4

Firmware Architecture for Embedded Systems:
Super Loop, Interrupt driven, RTOS, CMSIS RTOS, Low Power Operations. Speed Power Product, Optimisation for time and space.

Module 5

Debugging Techniques for Embedded Systems:
Introduction to GNU Debugger gdb. uVision IDE based debugging techniques. Single Stepping, Break Points, Watch Points, and Memory Probing. Simulation using uVision.

Lab Prerequisite:
Any ARM Cortex M0-4 microcontroller development board on Windows-7 or above platform, Kiel uVision MDK IDE. C compiler on Windows, preferably Cygwin. USB to Serial devices. Lab and Theory sessions are integrated.

Lab Work: 2 hrs/week

Course Outcomes:

At the end of the laboratory work, students will be able to:

- Use Embedded programming language like Embedded C and Scripting Language like Python
- Design and Use Cortex-Mx Microcontroller based embedded Systems

List of Experiments:

Many more lab experiments based on each topic and peripheral. Study datasheet and technical reference manual of case-study Cortex-Mx microcontroller.

1. Install Keil MDK for ARM along with development board drivers. Interface development board to development PC. Download and test blinky code example.
2. Develop a super loop to transmit ADC data on UART to PC every one second.
3. Develop a interrupt routine to accept 100 bytes of data from PC over UART and send out on SPI or I2C bus. Consider buffering and non-buffering approaches.
4. Utilize CMSIS RTOS and develop a user interface console with keyboard, display and any serial interface protocol.
5. Transfer periodically sampled data from any analog peripheral to either PC or another analog peripheral using DMA process. Code could be standalone or CMSIS based.
6. Develop Python code to interface external peripherals connected to PC.
7. Send emails using Python program.
8. Post data on to any webpage using Python.

9. Read data from webpage Python program and transfer the same to microcontroller over UART.
10. Receive data from microcontroller on to PC using Python and either email that data or post it on to any webpage.

Reference Books:

1. Joseph Yiu, "Definitive guide to the ARM Cortex-M3", Latest available edition

2. Hennessy and Patterson, "Computer Architecture: A Quantitative Approach", Latest available edition

3. Shibu K V, "Introduction to Embedded Systems", Latest available edition

4. Michael J Pont, "Embedded C", Latest available edition

5. Leonard Eddison, "Python Programming", Latest available edition

6. Technical reference manual and datasheets of Cortex-M3 microcontroller and other components.

And many other online tutorials and references.

Analog IC design

COURSE CODE	**18ECVEPCAI**	**COURSE TITLE**	**Analog IC design**
CREIDTS	**3**	**L-T-P**	**3-0-0**

CO-No	**Course Outcomes**	**PO**
CO1	Develop efficient analytical tools for quantifying the Analog circuits by inspection, aiming Analog design octagon**.**	**PO3**
CO2	Design stable Analog Integrated Circuits to meet given specification	**PO3**
CO3	Demonstrate Different Operational amplifier topologies through literature survey in groups.	**PO1,2**

Module 1

MOS I/V Characteristics, second order effects, MOS device models. Basics of single stage amplifiers

Module 2

Design and Analysis of Gain, Input, output Impedance of single stage amplifiers, frequency response of Common-Source and Source Follower

Module 3

Differential Amplifiers: Design and analysis of Differential Amplifiers for a given specification.

Module 4

Current Mirrors current mirrors, Cascade mirrors and active current mirrors

Noise: Types of noise, Noise in Single stage amplifier, Noise bandwidth

Module 5

Design of Two Stage Operational amplifier, Folded Cascode Operational amplifier, Telescopic operational amplifier

Reference Book:

1. "**Design of Analog CMOS Integrated Circuits**", Behzad Razavi, TMH, 2007.

2. Paul. R.Gray, Robert G. Meyer**, "Analysis and Design of Analog Integrated Circuits", Wiley, (4/e), 2001**

I Semester electives

Static Timing Analysis

COURSE CODE	**18ECVEPEST**	**COURSE TITLE**	**Static Timing Analysis**
CREIDTS	**3**	**L-T-P**	**3-0-0**

CO	Description	**PO**
CO1	Ability to **apply** the learnt basic concepts of STA to evaluate the delay of the circuits and **analyse** the generated report to identify critical issues and bottleneck for the violation and **suggest** the techniques to make the design to meet timing	**PO3**
CO2	Ability to **write** their own constraint file and create the environment required for the given design and its specification to undergo for **analysis using the EDA tool.**	**PO2**
CO3	Ability to understand the **journal research papers related to Timing analysis techniques** and able to present suitable techniques for the given design.	**PO1**

Module 1
Introduction: Basics of timing concepts
Delay Concepts for Digital Designing: Types of Delays in Digital Circuits, Different Cause for Delay

Timing parameters of digital circuits: Timing Parameters for Combinational Logic Gates, Timing Parameters for Sequential Circuits, Concept of Delay Path in a Design,Clock Concepts

Module 2
Resources for Static Timing Analysis Flow: Libraries, Netlist, Parasitics for Delay Calculation: Device Parasitics, Interconnects, Parasitics Extraction Formats, linear v/s. non-linear delay model

Module 3
Concepts of Noise and Crosstalk for static timing Analysis: Coupling Capacitance Concept, Type of Crosstalk Noise or Glitch, Types of Crosstalk Delta Delay, Noise Libraries, Crosstalk Effect on Timing Analysis, Strategy of Crosstalk on Nanometre Design: Cause for Crosstalk on Integrated Circuits, Crosstalk Prevention Methods.

Module 4
Constraints for STA: Clock Constraints, Other Timing Constraints, 5.2.2 External Delays of DUA, Timing Exceptions: Multicycle Path, False Path, Clock Grouping, Case Analysis, Disable Timing, Path with Derate

Module 5

Timing Violations and Verification: Slack, Critical Path of Timing Report,Setup Violation, Hold Violation, Multicycle Path, Half Cycle Path, Timing Checks for Asynchronous Timing Paths, Recovery and Removal Violation Check, Input/Output Timing Path Checks ,DRC Violation Check,Multi Speed Clock Domain, Crosstalk Checks, Techniques to Fix Timing Violation: Techniques to Fix Setup Violations, Techniques to Fix Hold Violations

References:

1. "Static Timing Analysis for Nanometer Designs: A Practical Approach", J. Bhasker, R. Chadha, Springer, 2009.
2. "Static Timing Analysis for VLSI circuits", R.Jayagowri, Pushpendra S. Yadav, MEDTECH, A Division of Scientific International , 2018.

Low Power VLSI Design

COURSE CODE	18ECVEPELP	COURSE TITLE	Low Power VLSI Design
CREIDTS	3	L-T-P	3-0-0

CO	Course Outcomes	PO
CO1	Ability to extend the knowledge on basics of MOSFETs and Power Dissipation in MOS circuits to obtain the concepts of different techniques for power optimization.	PO3
CO2	Ability to use the EDA tool to implement the designed circuit with techniques of power optimization in the design and justify obtained report by class room presentation.	PO2
CO3	Ability to understand the journal research papers related to low power and updates their knowledge for new techniques to incorporate in projects of the specified stream.	PO1

Module 1

Sources of Power dissipation: Dynamic Power Dissipation -Short Circuit Power, Switching Power, Glitching Power, Static Power Dissipation, Degrees of Freedom.

Module 2

Supply Voltage Scaling Approaches: Device feature size scaling Multi-Vdd Circuits Architectural level approaches: Parallelism, Pipelining Voltage scaling using high-level transformations Dynamic voltage scaling Power Management.

Module 3

Switched Capacitance Minimization Approaches: Hardware Software Tradeoff Bus Encoding Two's complements Vs Sign Magnitude Architectural optimization Clock Gating Logic styles.

Module 4

Leakage Power minimization Approaches: Variable-threshold-voltage CMOS (VTCMOS) approach Multi-threshold-voltage CMOS (MTCMOS) approach Power gating Transistor stacking Dual-V_t assignment approach (DTCMOS).

Module 5

Special Topics: Adiabatic Switching Circuits Battery-aware Synthesis Variation tolerant design CAD tools for low power synthesis

Text

1. Pal, Ajit, Low-Power VLSI Circuits and Systems, Springer publisher, 2015

Reference

1. Anantha P. Chandrakasan and Robert W. Brodersen, Low Power Digital CMOS Design, Kluwer Academic Publishers, 1995.
2. Kaushik Roy and Sharat C. Prasad, Low-Power CMOS VLSI Design, Wiley-Inter science, 2000.
3. NPTEL http://nptel.iitm.ac.in Computer Science and Engineering, Department of Computer Science and Engineering ,IIT Kharagpur

Advanced Computer Architecture

COURSE CODE	18ECVEPECA	COURSE TITLE	Advanced Computer Architecture
CREIDTS	3	L-T-P	3-0-0

CO	Course Outcomes	PO
CO1	Acquire knowledge on the basic concepts of computer design, identifying the performance parameters and quantitative principles. Recognize the instruction level parallelism and different methods used for scheduling and structuring the code. Understand the memory hierarchy, the I/O system and their impacts on system development. Analyse the performance and Identify the limitations of ILP for the efficiency of multi pipeline architecture. Recognize the performance improvements by implementing shared memory and cache coherence and Identify associated issues in Inter-processor communication.	PO3
CO2	Make a report of the selected topic and able to present it	PO2

Module1

Introduction and Review of Fundamentals of Computer Design: Introduction; Classes computers; Defining computer architecture; Trends in Technology; Trends in power in Integrated Circuits; Trends in cost; Dependability, Measuring, reporting and summarizing Performance; Quantitative Principles of computer design.

Pipelining, Instruction –Level Parallelism, Exploitation and Limits on ILP: Introduction to pipelining, ILP; Crosscutting issues, fallacies, and pitfalls with respect to pipelining; Basic concepts and challenges of ILP.

Module 2

Memory Hierarchy Design, Storage Systems: Review of basic concepts; Crosscutting issues in the design of memory hierarchies; Case study of AMD Opteron memory hierarchy; Fallacies and pitfalls in the design of memory hierarchies.

Module 3

Advanced topics in disk storage: Designing and evaluating an I/O system – The Internet archive cluster; Case study of NetAA FAS6000 filer; Fallacies and pitfalls Definition and examples of real faults and failures; I/O performance, reliability measures, and benchmarks**,** Queuing theory; crosscutting issues.

Module 4

Hardware and Software for VLIW and EPIC Introduction: Exploiting Instruction-Level Parallelism Statically, Detecting and Enhancing Loop-Level Parallelism, Scheduling and Structuring Code for Parallelism.

Module 5

Large-Scale Multiprocessors and Scientific Applications Introduction, Inter processor Communication: The Critical Performance Issue, Characteristics of Scientific Applications, Synchronization: Scaling Up, Performance of Scientific Applications on Shared-Memory Multiprocessors, Performance Measurement of Parallel Processors with Scientific Applications.

References:

1. John L. Hennessey and David A. Patterson, "**Computer Architecture – A quantitative approach",** Morgan Kaufmann / Elsevier, Fifth edition, 2012.
2. Richard Y. Kain, "**Advanced Computer Architecture a Systems Design Approach**", PHI, 2011

Embedded Computing and networking

COURSE CODE	18ECVEPEEC	COURSE TITLE	Embedded Computing and networking
CREIDTS	3	L-T-P	3-0-0

CO1	**Understand** different types of Embedded Applications. Analyse various development tools, WAN, LAN and PAN protocols. Customize Linux for different environment. Port OS to embedded board and to build Arm tool Chain	**PO3**
CO2	Make an effective presentation of the selected topic	PO2

Module 1

Types of embedded application: Super loop, Interrupt driven, priority, round robin, OS based.

Embedded Android: Android Mobile and Tablet**,** Android TV, Android Wearable, Android Auto, Glass.

WAN : MPLS, HHTP, MQTT, Coap etc

LAN: TCP / IP, UDP, Socket Programming

PAN: Bluetooth, BLE, zigbee

Module 2

Introduction to Software Development Tools: GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools.

Module 3

Interfacing Modules: Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, OpenCV for machine vision, Audio signal processing.

Module 4

Building an Embedded System: Creating the Root File system, Building the Linux Kernel, Building the Root File system, Running UML, Networking.

Module 5

Embedded ARM Devices: Building ARM tool chain, Installing an Operating System on ARM board, Using ARM board Serial Port, Remote Serial Port.

Text books:

1. Modern Embedded Computing - Peter Barry and Patrick Crowley, 1st Ed., Elsevier/Morgan Kaufmann, 2012.
2. Linux Application Development - Michael K. Johnson, Erik W. Troan, Adission Wesley, 1998.
3. Assembly Language for x86 Processors by Kip R. Irvine

4. Embedded Operating System - Alan Holt, Chi-Yu Huang, Springer
5. Intel® 64 and IA-32 Architectures Software Developer Manuals

Reference books:

1. Operating System Concepts by Abraham Silberschatz, Peter B. Galvin and Greg Gagne.
2. The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall
3. UNIX Network Programming by W. Richard Stevens

Device Modeling and Processing Technology

COURSE CODE	**18ECVEPEMP**	**COURSE TITLE**	**Device Modeling and Processing Technology**
CREIDTS	**3**	**L-T-P**	**3-0-0**

CO	Course Outcomes	PO
CO1	**Comprehend** fundamentals of semiconductors, theoretical and practical aspects of electronics technology – Very Large Scale Integration. All the unit process steps involved in planar process starting from silicon crystal growth to CMOS Process. Analyse SPICE Models of Diodes, BJT, MOSFETs, MESFETs & HBTs.	**PO3**
CO2	Ability to submit a report on the SPICE models fabrication process	**PO2**

Module 1

Fundamentals: Semiconductor Physics, Principle of circuit simulation and its objectives.

Introduction to SPICE: AC, DC, Transient, Noise, Temperature extra analysis.

Junction Diodes: DC, Small signal, large signal, High frequency and noise models of diodes, Measurement of diode model-parameters.

Module 2

Modelling of BJT: DC, small signal, high frequency and noise models of bipolar junction transistors. Extraction of BJT model parameters.

Module 3

MOSFETs: DC, small signal, high frequency and noise models of MOSFETs, MOS Capacitors. MOS.

Module 4

Models: Level-1 and level-2 large signal MOSFET models. Introduction to BSIM models. Extraction of MOSFET model parameters.

JFET, MESFETs & HBTs: Modelling of JFET & MESFET and extraction of parameters. Principles of hetro-junction devices, HBTs, HEMT.

Module 5

CMOS Processing Technology: An overview of wafer fabrication, Wafer Processing – Oxidation – Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – Interconnects circuit elements.

Text Books

1. S.M.Kang & Y.Leblibici, CMOS Digital Integrated Circuits-Analysis & Design, TMH, 3rd Ed.

2. S.M. Sze, Physics of Semiconductor Devices, Wiley Pub.

3. Neil H E Weste, David Harris, Ayan Banerjee, CMOS VLSI Design 3rd edition, Pearson Education.

References

1. Sedra and Smith, SPICE.

2. H.M. Rashid, Introduction to PSPICE, PHI.

3. B.G. Streetman & S. Baneerjee, Solid State Electronic Devices, PHI.

4. R. Raghuram, Computer Simulation of Electronic Circuits, Wiley Eastern Ltd.

Advances in VLSI Structure

COURSE CODE	**18ECVEPEAV**	**COURSE TITLE**	**Advances in VLSI Structure**
CREIDTS	**3**	**L-T-P**	**3-0-0**

CO	Description	PO
CO1	Ability to understand multiple-gate MOSFET's. Strained-Si technology, thin body MOSFET's and Emerging nano materials. Apply the short channel effect to define new structures and requirement of new materials. Analyse thin body MOSFET structure and its impact, Impacts of substrate; nano materials	PO3
CO2	Use modern tool to simulate different structure and observe the performance comparison and make an effective documentation	PO2

Module 1

Transistor and multiple-gate MOSFET's development, history, review of MOSFET principles and performance metrics

Module 2

Issues in short-channel MOSFET electrostatics; scale length fundamentals for thin-body MOSFETs (FinFET, planar Fully-Depleted SOI MOSFET and Gate-All-Around MOSFET)

Module 3

Advantages of thin body MOSFET's electrostatics quantum mechanical effects; effective carrier mobility; high-field velocities. Parasite resistance; thin-body MOSFET's carrier transport MOSFET compact modelling and Technology CAD (TCAD)

Module 4

Impacts of substrate; Fin shape tuning; Gate stack process, FinFET's source/drain process, Multiple-gate MOSFET's threshold voltage engineering. Multiple-gate MOSFET performance dependence on channel orientation and strain

Strained-Si technology and its effectiveness on Multiple-gate MOSFETs high-mobility channel transistors (Group III-V)

Module 5

Emerging nano materials: Nanotubes, nanorods and other nano structures, MOSFET like structure of carbon nano tubes.

Reference:

1. Research papers
2. **MOOC**: http://www.flexilearn.ie/course/Nanoelectronics/43

RESEARCH METHODOLOGY

COMPULSORY TO ALL BRANCHES

COURSE CODE	**18ALLPICRM**	**COURSE TITLE**	**RESEARCH METHODOLOGY**
CREIDTS	**2**	**L-T-P**	**2-0-0**

CO	**Course Outcomes**	**PO**
CO1	Ability to write and present a substantial technical report/document	PO2
CO2	Able to demonstrate a degree of mastery over the area of specialization	PO3

Module 1:

Meaning and sources of research problem, , Objectives and Characteristics of research – Errors in selecting research problem, Research methods Vs Methodology - Types of research-Criteria of good research – Developing a research plan.

Module 2:

Investigations of a research problem - Selecting the problem - Necessity of defining the problem – Data collections-analysis- Importance of literature review in defining a problem - Survey of literature -Necessary instrumentations

Module 3:

How to write paper-conference articles-poster preparation, thesis report writing, inclusion of references, journal reviewing process, journal selection process, filling about journal template, developing effective research proposal-plagiarism-research ethics

Module 4:

Nature of Intellectual property, IPRs- Invention and Creativity - Importance and Protection of Intellectual Property Rights (IPRs) – procedure for grant of patents and patenting under PCT-types of patents-technological research and innovation- international cooperation on IP.

Module 5:

A brief summary of : Patents-Copyrights-Trademarks, patent rights-licensing and transfer of technology-patent databases-case studies on IPR-Geographical indications-new developments in IPR-protection of IPR rights

REFERENCE BOOKS:

1. Garg, B.L., Karadia, R., Agarwal, F. and Agarwal, U.K., 2002. An introduction to Research Methodology, RBSA Publishers.
2. Kothari, C.R., 1990. Research Methodology: Methods and Techniques. New Age International. 418p.
3. Anderson, T. W., An Introduction to Multivariate Statistical Analysis, Wiley Eastern Pvt., Ltd., New Delhi
4. Sinha, S.C. and Dhiman, A.K., 2002. Research Methodology, Ess Ess Publications. 2
5. Subbarau NR-Handbook of Intellectual property law and practise- S Viswanathan Printers and Publishing Private Limited 1998.

II SEMESTER

Program Core Course Syllabus

II SEMESTER

Program Core Course Syllabus

Mixed Signal Circuit Design

COURSE CODE	**18ECVEPCMS**	**COURSE TITLE**	**Mixed Signal Circuit Design**
CREIDTS	**4**	**L-T-P**	**3-0-1**

CO-	Course Outcomes	PO
CO1	Demonstrate Transceiver basic building blocks like PLL, Data converters, Sample and hold circuit.	**PO3**
CO2	Design and simulation of identified blocks of Transceiver and submit a technical report	**PO2,3**

Prerequisite: Data converter fundamentals

Module 1

Feedback amplifier: Types, topologies, Effect of Feedback on noise,

Module 2

Oscillators, VCO: General consideration, Ring oscillator, LC oscillator, Voltage Controlled oscillator.

Module 3

PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications.

Module 4

Switched capacitor circuits, Sampling switches, Switched capacitor Amplifiers.

Module 5

Study of errors in Data converters

Reference Book:

1. "Design of Analog CMOS Integrated Circuits", Behzad Razavi, TMH, 2007.

2. CMOS: Circuit Design, Layout, and Simulation, 3rd Edition –R. Jacob baker.

3. Roubik Gregorian: Introduction to CMOS Op-amps and comparators, Wiley.

4. David A Johns, Ken Martin: Analog IC design, Wiley 2008.

Lab Experiments:

Lab Work: 2 hrs/week

Course Outcomes:

At the end of the laboratory work, students will be able to:

- Design digital Circuit using CMOS Technology
- Use EDA tools like Cadence, Synopsis, Mentor Graphics to simulate and measure performance parameters of Analog and Mixed Signal circuits

List of Experiments:

1) Design and Analyse frequency response (Phase Margin, gain Margin) and noise for the following circuits for a given specification,

a) Two Stage Operational amplifier,

b) Folded Cascode Operational amplifier,

c) Telescopic operational amplifier

2) **Design** sub blocks of PLL and measure all the parameters.
3) **Design** a simple ADC/DAC and analyse

Design for Testability

COURSE CODE	**18ECVEPCDT**	**COURSE TITLE**	**Design for Testability**
CREIDTS	**4**	**L-T-P**	**3-1-0**

CO	Description	**PO**
CO1	Apply the concept of faults and failure models to generate the number of fault models & Automatic Test Pattern Generator (ATPG) for the given design under test (DUT). Analyze and identify the given fault in given DUT(can be logic circuit or memory) and conclude the suitable available solution to test these faults. Ability to generate the Automatic Test Pattern Generation (ATPG) with different techniques using EDA tool	**PO3**
CO2	Engage on Literature survey and make an effort to suggest new solution as a team	**PO1, 2**

Module 1

Introduction to Testing

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

Module 2

Logic and Fault Simulation

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG. Fault

Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits, Detection of Multiple Faults in Combinational Logic Circuits.

Module 3

Testability Measures

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

Module 4

Built-In Self-Test

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST.

Module 5

Boundary Scan Standard

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Power issues in IC Testing

Text books:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L.Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

Reference books:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, JaicoPublishing House.

2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

Real Time Operating Systems

COURSE CODE	**18ECVEGCRT/ 18ECELGCRT**	**COURSE TITLE**	**Real Time Operating Systems**
CREIDTS	**4**	**L-T-P**	**3-0-1**

CO1	Design high performance software applications with real time deterministic response.	**PO3**
CO2	Configure and Optimize Embedded RTOS to achieve desired High Performance Computing response.	**PO3**

CO3	Make an effective oral presentation pertaining to RTOS and related high performance computing concepts.	**PO2**
CO4	Engage on Literature survey about High Performance & Deterministic systems, both from hardware and software perspective and submit a report	**PO1**

Module 1
Basic concepts of RTOS: Defining RTOS, characteristics of RTOS, objects and services, real time scheduling approaches, Library-Based RTOS (Kernel-less approach), monolithic kernels, microkernels, virtual machines.

Module 2
RTOS objects: Tasks and task states, Semaphores: need, types, typical operations, mutual exclusion, priority inversion avoidance. **Queues:** States, typical operations, non-interlocked one way data communication, no-interlocked and interlocked two way data communication, broadcast data communication, Queues within an Interrupt Service Routine,

Module 3
RTOS objects:
Critical Sections and Resource Management, **Pipes:** Pipe states, pipe control blocks, typical operations, uses of pipes

Module 4
RTOS services: TCP/IP communication, client server model, sockets and ports, exception handling, interrupt mechanism

Module 5
Comparison of available RTOS, Selection criteria of an RTOS for an IoT application
Application implementation: Process of designing firmware, boot loader, device drivers, developing interface code for module developed for any hardware: C program-based application layer code and kernel level code to configure and access data in/out of any chosen hardware.

References:

- Embedded and real time operating systems by Wang, K.C., Springer 2017, ISBN-10 : 3319515160 and ISBN-13 : 9783319515168
- Real-Time Concepts for Embedded Systems by Qing Li and CarolynYaoISBN:1578201241
  CMP Books
  NPTEL lectures on 'Real Time Systems'
- Mastering embedded Linux programming by Chris Simmonds Publisher: Packt Publishing, 2017 ISBN: 9781787283282 **OR**
- Using the free RTOS Real Time Kernel by Richard Barry, http://www.FreeRTOS.org

Lab exercises: (Can be implemented using any RTOS and any hardware)
- Task creation, priority assignment, scheduling, deletion (Verify/design scheduling algorithms and check its efficiency)
- Resource management: Semaphores and mutexes, priority inversion
- Queue management
- Interrupt management

II Semester electives

II Semester electives

System Verilog and Verification

COURSE CODE	**18ECVEPESV**	**COURSE TITLE**	**System Verilog and Verification**	
CREIDTS	**4**	**L-T-P**	**3-0-0**	

CO-No	Course Outcomes	PO
CO1	Define, Understand and Explain OOPs concepts and system Verilog data types, Apply system Verilog constructs to create verification environment, Analyse coverage driven verification for given design under test(DUT)	**PO3**
CO2	Able to conceptualize and obtain 100% code coverage and functional coverage by determining the set of input constraints and assertions in test benches and able to document the effort to obtain coverage	**PO2,3**

Module 1

Verification Concepts: Concepts of verification, importance of verification, Stimulus vs Verification, functional verification, test bench generation, functional verification approaches, typical verification flow, stimulus generation, direct testing, Coverage: Code and Functional coverage, coverage plan.

Module 2

System Verilog: System Verilog constructs - Data types: two-state data, strings, arrays: queues, dynamic and associative arrays, Structs, enumerated types. Program blocks, module, interfaces, clocking blocks, modports.

Module 3

System Verilog: SV Classes: Language evolution, Classes and objects, Class Variables and Methods, Class instantiation, Inheritance, and encapsulation, Polymorphism.

Randomization: Directed Vs Random Testing. Randomization: Constraint Driven Randomization.

Module 4

System Verilog: Assertions, Introduction to Assertion based verification, Immediate and concurrent assertions.

Coverage driven verification: Motivation, Types of coverage, Cover Group, Cover Point, Cross Coverage, Concepts of Binning and event sampling.

Building Test bench: Layered test bench architecture.

Module 5

Introduction to Universal Verification Methodology, Overview of UVM Base Classes and simulation phases in UVM and UVM macros. Unified messaging in UVM, UVM environment structure, Connecting DUT- Virtual Interface

References:

1. Janick Bergeron, Writing Testbenches Using SystemVerilog
2. Chris Spear, SystemVerilog for Verification
3. Janick Bergeron, Eduard Cerny, Alan Hunter, and Andy Nightingale, Verification Methodology Manual for SystemVerilog

Physical Design

COURSE CODE	**18ECVEPEPD**	**COURSE TITLE**	**Physical design**
CREIDTS	**3**	**L-T-P**	**3-0-0**

CO	Course Outcomes	PO
CO-1	Demonstrate the basic design flow in VLSI physical design automation and the basic algorithms used for implementing the same	**PO3**
CO-2	Make an Effective Documentation of Physical Design Flow using industry level EDA tool.	**PO2**

Module 1

Physical design flow, Libraries and File Formats. Introduction to physical design automation, Physical Design flow, EDA tools, Input files, Libraries: Standard Cells, Transistor Sizing, Input-Output Pads, Library Characterization, Constraints based design, File formats:Library Exchange Format (LEF), DEF (Design Exchange Format), Liberty Timing File (LIB).

Module 2

Partitioning and floor planning. Partitioning Techniques, Classification of Partitioning Algorithms, Floor planning, Design Style Specific Issues, macro placement, Floor planning Algorithms.

Module 3

Placement: Design Style Specific Placement Problems, Goals of placement, and Sanity checks before placement. Classification of Placement algorithms, Simulation Based Placement Algorithms: Simulated Annealing, Force Directed Placement, Interconnection Topologies, Estimation of Wire length.

Module 4

Clock Tree Synthesis and Timing Analysis. Sanity checks before CTS. Need and goals of CTS. CTS related Terminologies. Clock skew reduction techniques and Topologies. Clock buffering mechanism. Post CTS Optimization. Basic timing related quantities.

Module 5

Routing and signoff checks, Goals of Routing, Routing Prerequisites, Routing Constraints, Global Routing, Track Assignment, Detail Routing, Routing algorithms. Design Rule Check (DRC), Layout versus Schematic (LVS), commonly faced LVS issues, IR Drop Analysis: Static IR drop analysis, Dynamic IR drop analysis, Methods to reduce IR drop: ELECTRO MIGRATION (EM): Methods to fix EM

Text Book

- Khosrow Golshan,"Physical Design Essentials-An ASIC Design Implementation Perspective", 2007 Springer Science+Business, Media
- Sherwani, Naveed A. "Algorithms for VLSI Physical Design Automation"

Reference books:

- Sarafzadeh, C.K. Wong, "An Introduction to VLSI Physical Design", McGraw Hill International Edition 1995.
- Preas M. Lorenzatti, " Physical Design and Automation of VLSI systems", The Benjamin Cummins Publishers, 1998.

Hardware-Software Co-design

COURSE CODE	**18ECVEPEHS**	**COURSE TITLE**	Hardware-Software Co-design
CREIDTS	**3**	**L-T-P**	**3-0-0**

CO	Course Outcomes	PO
CO-1	Understand fundamental issues in co-design, Learn about prototyping and emulation, Understand compilation techniques, and learn related tools. Acquire ability to differentiate various target architectures.	PO3
CO-2	Acquire ability to generate specifications and develop verification plans and make a documentation.	PO2

Module 1

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

Module 2

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Module 3

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

Module 4

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

Module 5

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

Text books:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.

2. Hardware / Software Co- Design - Giovanni De Micheli Maria Giovanna Sami, 2002, Kluwer Academic Publishers

Reference books: 1. A Practical Introduction to Hardware/Software Co-design - Patrick R. Schaumont - 2010 – Springer

System on Chip Architecture

COURSE CODE	18ECVEPESC	COURSE TITLE	System On Chip Architecture
CREIDTS	3	L-T-P	3-0-0

CO	Course Outcomes	PO
CO1	**Apply** concepts of Moore's law, CMOS scaling to understand the System on Chip with its need, evolution, challenges, goals, superiority over system on board & stacked ICs in package. **Analyze** Typical goals in SoC design and also inter connect architecture	**PO3**
CO2	**Design** solutions for issues at system level, and issues of Hardware-Software co design and make an effective presentation.	**PO2**

Module 1

Review of Moore's law and CMOS scaling, benefits of System On Chip integration in terms of cost, power, and performance. Comparison on System on Board, System on Chip, and System-in-Package. Typical goals in SoC design cost reduction, power reduction, design effort reduction, performance maximization. Productivity gap issues and the ways to improve the gap – IP based design and design reuse.

Module 2

System On Chip Design Process: A canonical SoC Design, SoC Design flow, waterfall vs spiral, top down vs bottom up, Specification requirement, Types of Specification, System Design Process, System level design issues, Soft IP vs Hard IP, IP verification and Integration, Hardware-Software co design, Design for timing closure, Logic design issues, Verification strategy, On chip buses and interfaces, Low Power, Hardware Accelerators in Soc.

Module 3

Embedded Memories, cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence. MESI protocol and Directory-based coherence.

Module 4

Interconnect architectures for SoC. Bus architecture and its limitations. Network on Chip (NOC) topologies. Mesh-based NoC. Routing in an NoC. Packet switching and wormhole routing.

Module 5

MPSoCs: What, Why, How MPSoCs, Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design

Case Study: A Low Power Open Multimedia Application Platform for 3G Wireless.

Reference Books:

1. Sudeep Pasricha and Nikil Dutt,**"On-Chip Communication Architectures: System on Chip Interconnect"**, Morgan Kaufmann
Publishers © 2008.
2. Rao R. Tummala, Madhavan Swaminathan, **"Introduction to system on package sop-Miniaturization of the Entire Syste"**,
McGraw-Hill, 2008.
3. James K. Peckol, **"Embedded Systems: A Contemporary Design Tool"**, Wiley Student Edition.
4. Michael Keating, Pierre Bricaud, **"Reuse Methodology Manual for System on Chip designs"**, Kluwer Accademic Publishers, 2nd
edition, 2008.
5. Sung-Mo Kang, Yusuf Leblebici, **"CMOS Digital Integrated Circuits"**, Tata Mcgraw-Hill, 3rd Edition.

Embedded design using ARM architecture

COURSE CODE	18ECVEPEAA	COURSE TITLE	Embedded design using ARM architecture
CREIDTS	3	L-T-P	3-0-0

CO1	**Acquire the knowledge** on ARM organization and the feature rich ARM Cortex architecture and to understand serial communication techniques with microcontroller. **apply** skills to model complete Embedded System.
CO2	**Analyze** digital and analog peripherals, memory of ARM Cortex-Mx microcontrollers
CO3	**Conduct experiments** with ARM Cortex board to develop various application
CO4	Ability to **Demonstrate** the development of embedded applications using ARM Cortex platforms, in a team or individual

Introduction to Embedded Systems, Microprocessors and Microcontrollers, RISC & ARM Architecture, Introduction to ARM Cortex – M Processor Family, Introduction to Software development process and platform.

Lab: Introduction to mbed/similar development board, Keil/similar IDE environment, Blinky Code, Key Input Single/linear/matrix, Interfacing character & graphic LCD.

ARM Cortex – M Architecture Programming Model, Instruction Set, Interrupts & Exception Handling, Timers & PWM

Lab: Experiments with Timers, Generation of 3 phase PWM, Sine wave generation, speed control of DC motor using PWM

Memory model, DMA, Floating Point Operations, Serial Communication peripherals: UART+SPI+I2C, Cortex Microcontroller Software Interface Standard

Lab: Interfacing two devices using UART, Read/Write Memory chip using SPI, Interface RTC chip using I2C

Analog peripherals ADC, DAC, interfacing analog sensors like, temperature, pressure sensors. Low power configurations of ARM microcontrollers

Lab: Generating waveforms using DAC, Acquiring analog signals using ADC and characterizing using FFT

DSP on ARM Cortex-M4, Developing Closed Loop & PID Control Systems

Lab: Interfacing with PC using Serial peripherals are using wireless devices

Reference Books:

1. Fast and Effective Embedded Systems Design: Applying the ARM mbed, by Rob Toulson & Tim Wilmshurst, Newnes, 2012

2. The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors, by Joseph Yiu, Newnes, 2013

3. The Designer's Guide to the Cortex-M Processor Family: A Tutorial Approach, by Trevor Martin, Newnes, 2013

Memory Design and Testing

COURSE CODE	**18ECVEPEMD**	**COURSE TITLE**	**Memory Design and Testing**
CREIDTS	**3**	**L-T-P**	**3-0-0**

CO1	Acquire the knowledge on Semiconductor memories, Apply the knowledge of CMOS technology and electronic circuits theory to design semiconductor memories, Analyze different types of memories**,** Apply the knowledge of CMOS technology and electronic circuits theory to design semiconductor memories	**PO3**
CO2	Ability to submit a report on the impact/growth of Advanced Memory Technologies for societal and sustained development.	**PO2**

Module 1

Random Access Memory Technologies: SRAM Cell Structures-MOS SRAM Architecture, MOS SRAM Cell and Peripheral, Circuit Operation, Bipolar SRAM Technologies, Silicon On Insulator (SOl) Technology, Advanced SRAM Architectures and Technologies, Application Specific SRAMs.

Module 2

Dynamic Random Access Memories (DRAMs): DRAM Technology Development, CMOS DRAMs, DRAMs Cell Theory and Advanced Cell Structures, BiCMOS DRAMs, Soft Error Failures in DRAMs, Advanced DRAM Designs and Architecture, Application Specific DRAMs.

Module 3

Non-volatile Memories: Masked Read-Only Memories (ROMs), High Density ROMs, Programmable Read Only Memories (PROMs), Bipolar PROMs, CMOS PROMs, Erasable (UV), Programmable Road-Only Memories (EPROMs), Floating-Gate EPROM Cell, One-Time Programmable (OTP) EPROMS, Electrically Erasable PROMs (EEPROMs), EEPROM Technology and Architecture, Non-volatile SRAM, Flash Memories (EPROMs or EEPROM), Advanced Flash Memory Architecture.

Module 4

Memory Fault Modelling, Testing and Memory Design For Testability and Fault Tolerance. RAM Fault Modelling, Electrical Testing, Pseudo Random Testing, Megabit DRAM Testing, Non-volatile Memory Modelling and Testing, IDDQ Fault Modelling and Testing, Application Specific Memory Testing.

Module 5

Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Non-volatile Memory Reliability, Reliability Modelling and Failure Rate Prediction. Design for Reliability, Reliability Test Structures, Reliability Screening and Qualification. Radiation Effects, Single Event Phenomenon (SEP), Radiation Hardening Techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test Structures.

Text Books

1. A.K Sharma, “Semiconductor Memories Technology, Testing and Reliability”, IEEE Press.
2. Luecke Mize Care, “Semiconductor Memory design & application”, Mc-Graw Hill.
3. Belty Prince, “ Semiconductor Memory Design Handbook”
4. Memory Technology design and testing 1999 IEEE International Workshop on: IEEE Computer Society Sponsor.

Open elective

MEMS & Microsystems

COURSE CODE	**18ECVEPEMM**	**COURSE TITLE**	**MEMS & Microsystems**
CREIDTS	**4**	**L-T-P**	**4-0-0**

CO	Description	PO
CO1	Understand the fundamentals of MEMS and its application, scaling, miniaturization, fabrication. Analyse the working of sensors, actuators and transducers. Design, modelling and packaging of micro systems	**PO3**
CO2	Able to make Documentation of Innovations in MEMS and Micro Systems	**PO2**

Module 1

Overview of MEMS & Microsystems: MEMS & Microsystems, Typical MEMS and Micro system products — features of MEMS, The multidisciplinary nature of Microsystems design and manufacture, Applications of Microsystems in automotive industry, health care industry, aerospace industry, industrial products, consumer products and telecommunications.

Module 2

Transduction Principles in MEMS & Microsystems: Introduction, Micro sensors — AW Sensors, thermal, Chemical, biomedical, optical, Pressure radiation, mechanical, magnetic, Micro actuation using thermal forces, piezo eclectic and electrostatic forces and shape-memory alloys. MEMS with micro actuators, microfluidics.

Module 3

Microsystems Fabrication Process: Introduction, Photolithography, Ion-implantation, diffusion, oxidation, CVD, PVD, etching and materials used for MEMS, Some MEMS fabrication processes: surface micro-machining, bulk micromachining, LIGA process, LASER micro machining.

Module-4

Micro System Design and Modelling: Introduction, Design considerations: Process design, Mechanical design.

Scaling Laws in Miniaturization: Introduction to scaling, scaling in geometry, scaling in rigid body dynamics, scaling electrostatic forces, electromagnetic forces, electricity, scaling in fluid mechanics & heat transfer.

Module-5

Micro system packaging: Over view of mechanical packaging of microelectronics micro system packaging, Interfaces in micro system packaging.

Wire bonding, Sealing of MEMS devices and various Packaging technologies.

III SEMESTER

Master of Technology
In
VLSI Design and Embedded system

Elective 5			
18ECVEGEUV	UVM Methodology concepts	18ECVEGESL	Introduction to scripting languages

Scripting Languages

COURSE CODE	18ECVEGESL	COURSE TITLE	Scripting Languages
CREDITS	3	L-T-P	2– 1 – 0

Overview of Scripting Languages – PERL, TCL, CGI, VB Script, Java Script. 8hrs
PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, 8

Inter process Communication Threads, Compilation & Line Interfacing. 9

UVM Methodology concepts

COURSE CODE	18ECVEGEUV	COURSE TITLE	UVM Methodology concepts
CREDITS	3	L-T-P	2– 1 – 0

Prerequisite: Introduction to Universal Verification Methodology, Overview of UVM Base Classes and simulation phases in UVM and UVM macros. Unified messaging in UVM, UVM environment structure, Connecting DUT- Virtual Interface

Over view of OVM Environment with OVM Libraries

Introduction to OVM, OVM and Coverage-Driven Verification (CDV), Test bench and Environments. OVC Overview. Data Item (Transaction). Driver (BFM). Sequencer. Monitor. Agent. Environment. The System Verilog OVM Class Library. OVM Facilities.

Transaction-Level Modeling (TLM). Transaction-Level Modeling Overview. TLM Basics. Transaction-Level Communication. Basic TLM Communication. Communicating Between Processes. Blocking versus Nonblocking. Connecting Transaction-Level Components. Peer-to-Peer connections. Port/Export Compatibility. Encapsulation and Hierarchy. Hierarchical Connections. Analysis Communication, Ports, Exports.

Developing Reusable Open Verification Components (OVCs)

Modelling Data Items for Generation. Inheritance and Constraint Layering. Defining Control Fields (“Knobs”). Transaction-Level Components. Creating the Driver. Creating the Sequencer. Connecting the Driver and Sequencer. Fetching Consecutive Randomized Items. Sending Processed Data Back to the Sequencer. Using TLM-Based Drivers. Creating the

Monitor. Instantiating Components. Creating the Agent. Creating the Environment. The Environment Class. The OVM Configuration Mechanism.

References

OVM User Guide, Version 2.1.2, © 2008–2011 Cadence Design Systems, Inc. (Cadence). All rights reserved. Cadence Design Systems, Inc., 2655 Seely Ave., San Jose, CA 95134, USA. © 2008–2011 Mentor Graphics, Corp. (Mentor). All rights reserved. Mentor Graphics, Corp., 8005 SW Boeckman Rd., Wilsonville, OR 97070, USA
http://www.specman-verification.com/source_bank/ovm-2.1.2/ovm-2.1.2/OVM_UserGuide.pdf

Verification Methodology Manual for System Verilog, © 2008–2011 Cadence Design Systems, Inc. (Cadence). All rights reserved.Cadence Design Systems, Inc., 2655 Seely Ave., San Jose, CA 95134, USA. © 2008–2011 Mentor Graphics, Corp. (Mentor). All rights eserved. Mentor Graphics, Corp., 8005 SW Boeckman Rd., Wilsonville, OR 97070, USA
http://read.pudn.com/downloads178/ebook/825398/vmm_sv.pdf

Course Title: Project work (phase-1)

COURSE CODE	18ECVEPWP1	COURSE TITLE	PROJECT WORK(Phase-1)
CREDITS	8	L-T-P	0 – 0 – 8

	Course Outcomes of phase-1	
CO1	Identify a suitable project by making use of the technical and engineering knowledge gained from previous courses with the awareness of impact of technology on the Society and their ethical responsibilities.	PO3
CO2	Collect and disseminate information related to the selected project within given time frame.	PO1
CO3	Communicate technical and general information by means of oral as well as written Presentation skills with professionalism.	PO2

Course Title: Internship

COURSE CODE	18ECVEPCIN	COURSE TITLE	INTERNSHIP
CREDITS	9	L-T-P	0 – 0 –9

	Course Outcomes of Internship	
CO1	Ability to develop a sound theoretical and practical knowledge of new technologies.	PO3
CO2	Ability to Develop domain specific problem solving and critical thinking skills, individual responsibility towards their internship goal as well as participate as an effective team member, to gain exposure to professional work culture & practices	PO3
CO3	Develop effective presentation & communication skills, and create proper documentation of the work	PO2

Course Title: Technical Seminar-1

COURSE CODE	18ECVESR01	COURSE TITLE	TECHNICAL SEMINAR-1
CREDITS	02	L-T-P-S	0 – 0 – 2

CO1	Identify the problem through literature survey by applying depth knowledge of the chosen domain	PO1,3
CO2	Analyse, synthesize and conceptualize the identified problem	PO3
CO3	Communicate clearly, write effective reports and make effective presentations following the professional code of conduct and ethics	PO2
CO4	Comprehensively study the domains and reflect the same towards the future enhancements of the work	PO2

Master of Technology

In

VLSI Design and Embedded system

IV SEMESTER

Course Title: Technical Seminar-2

COURSE CODE	18ECVESR02	COURSE TITLE	TECHNICAL SEMINAR-2
CREDITS	02	L-T-P	0 – 0 – 2

COURSE OUTCOMES

CO1	Identify the problem through literature survey by applying depth knowledge of the chosen domain	PO1,3
CO2	Analyse, synthesize and conceptualize the identified problem	PO3
CO3	Communicate clearly, write effective reports and make effective presentations following the professional code of conduct and ethics	PO2
CO4	Comprehensively study the domains and reflect the same towards the future enhancements of the work	PO2

PROJECT WORK (Phase-2)

COURSE CODE	18ECVEPWP2	COURSE TITLE	PROJECT WORK (Final-Phase)
CREDITS	20	L-T-P	0 - 0 – 20

	COURSE OUTCOMES(Phase-2)	
CO1	Identify the modern tools required for the implementation of the project.	PO3
CO2	Design, examine critically and implement or develop a prototype for the identified problem during Phase I	PO1
CO3	Communicate technical information by means of oral as well as written presentation skills with professionalism.	PO2